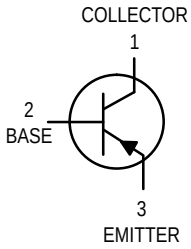
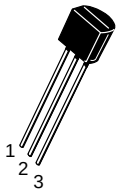
High Voltage Transistors

PNP Silicon

BC450,A





CASE 29–04, STYLE 17
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	–100	Vdc
Collector–Base Voltage	V_{CBO}	–100	Vdc
Emitter–Base Voltage	V_{EBO}	–5.0	Vdc
Collector Current — Continuous	I_C	–300	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

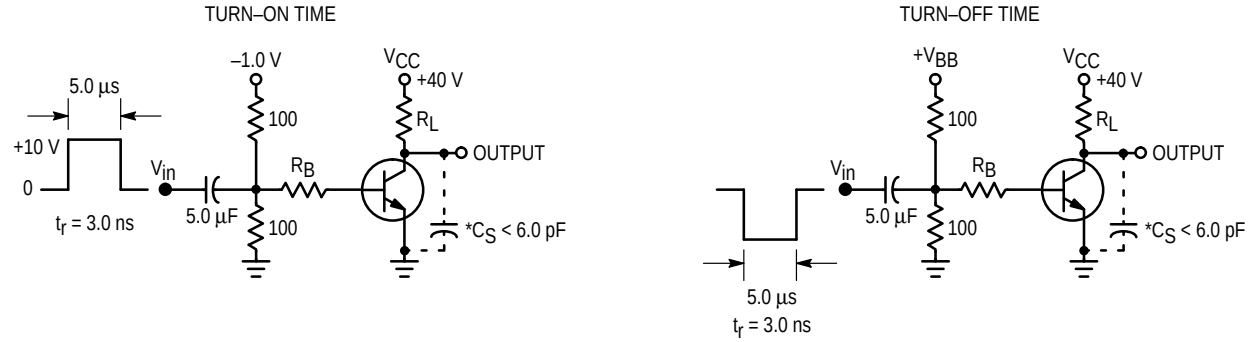
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage(1) (I_C = –1.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	–100	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = –100 μA, I_E = 0)		$V_{(BR)CBO}$	–100	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = –10 μAdc, I_C = 0)		$V_{(BR)EBO}$	–5.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = –80 Vdc, I_E = 0)		I_{CBO}	—	—	–100	nAdc
ON CHARACTERISTICS*						
DC Current Gain		h_{FE}				—
(I_C = –2.0 mA, V_{CE} = –5.0 V)	BC450		50	—	460	
	BC450A		120	—	220	
(I_C = –10 mA, V_{CE} = –5.0 V)	BC450		50	—	—	
	BC450A		100	—	—	
(I_C = –100 mA, V_{CE} = –5.0 V)	BC450		50	—	—	
	BC450A		60	—	—	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS(1) (Continued)					
Collector–Emitter Saturation Voltage (I_C = –100 mAdc, I_B = –10 mAdc)	$V_{CE(sat)}$	—	–0.125	–0.25	Vdc
Base–Emitter Saturation Voltage (I_C = –100 mAdc, I_B = –10 mAdc)	$V_{BE(sat)}$	—	–0.85	—	Vdc
Base–Emitter On Voltage (I_C = –2.0 mA, V_{CE} = –5.0 V) (I_C = –100 mA, V_{CE} = –5.0 V)*	$V_{BE(on)}$	–0.55 —	— –0.76	–0.7 –1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = –50 mAdc, V_{CE} = –5.0 Vdc, f = 100 MHz)	f_T	100	200	—	MHz

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle 2.0%.



* Total Shunt Capacitance of Test Jig and Connectors
For PNP Test Circuits, Reverse All Voltage Polarities

Figure 1. Switching Time Test Circuits

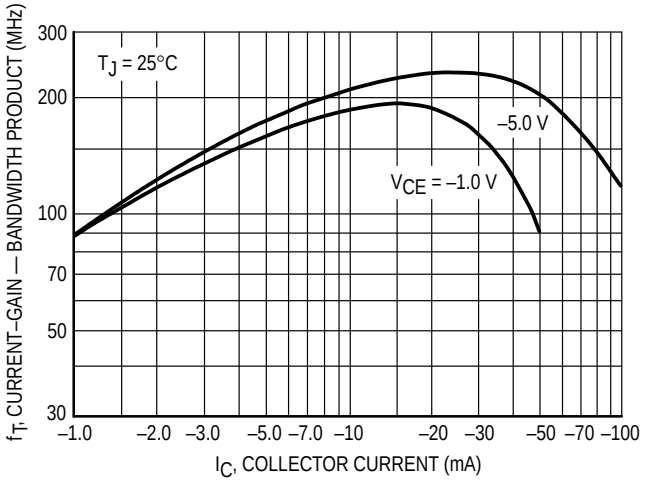


Figure 2. Current–Gain — Bandwidth Product

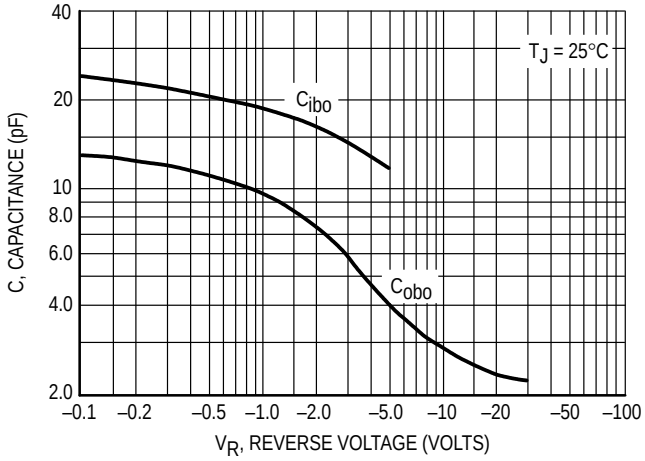


Figure 3. Capacitance

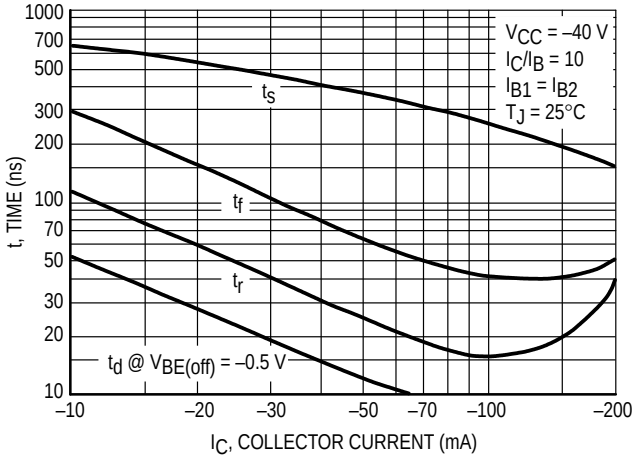


Figure 4. Switching Times

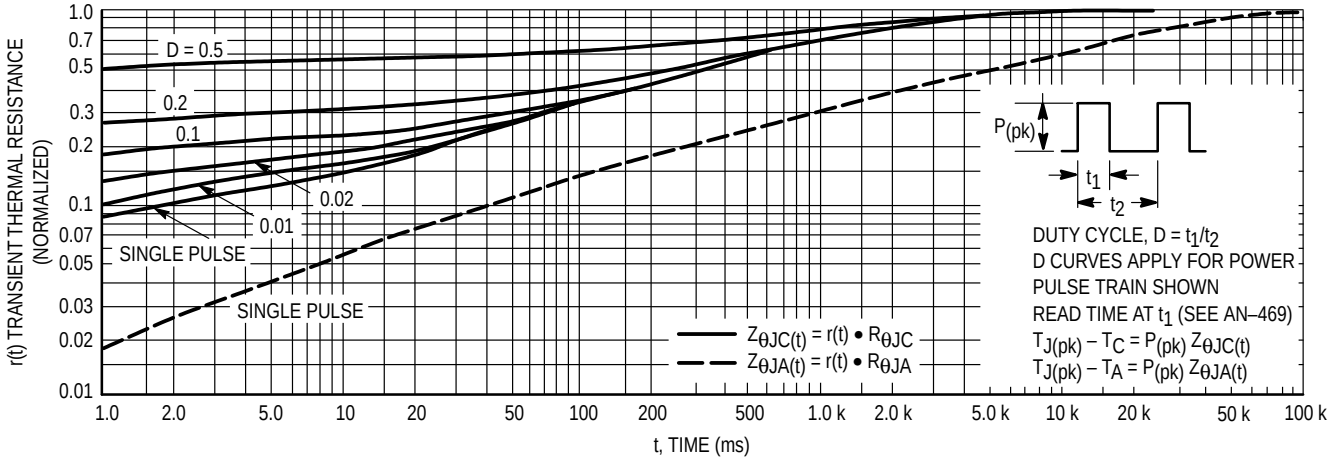


Figure 5. Thermal Response

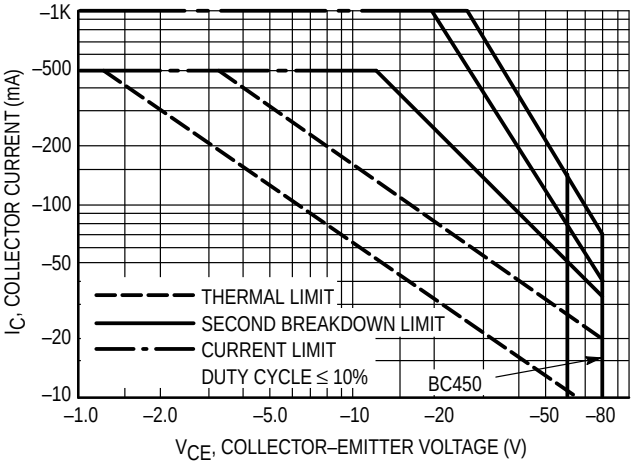


Figure 6. Active Region — Safe Operating Area

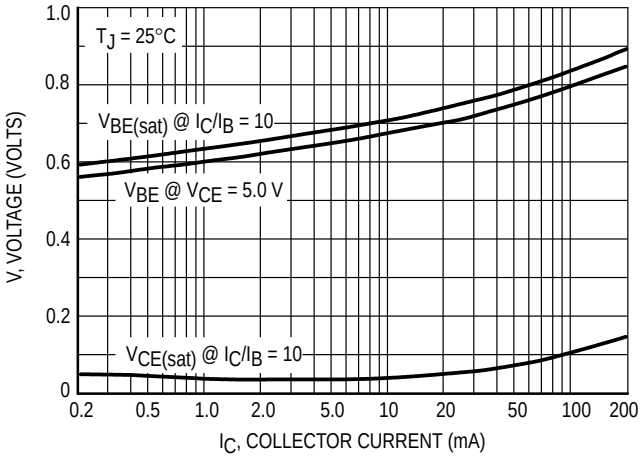


Figure 7. “On” Voltages

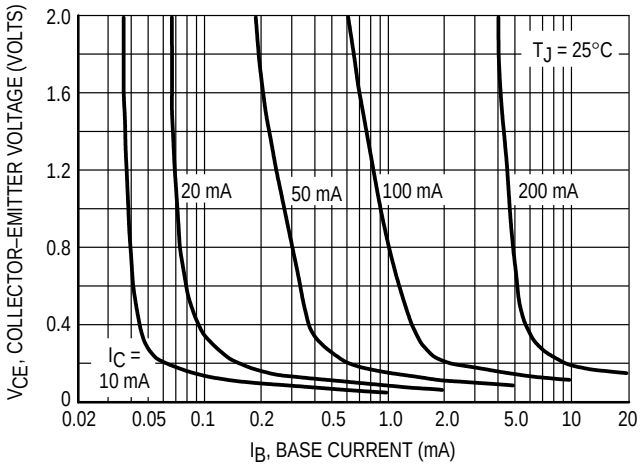


Figure 8. Collector Saturation Region

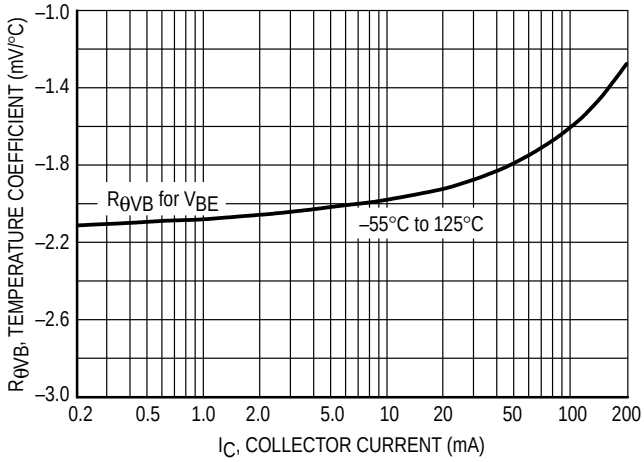


Figure 9. Base–Emitter Temperature Coefficient

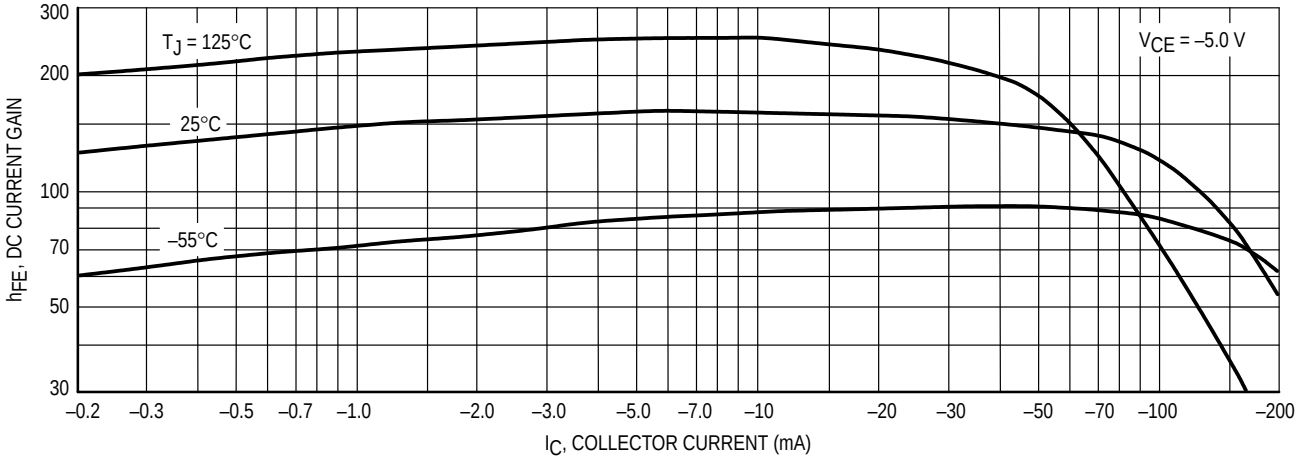


Figure 10. DC Current Gain

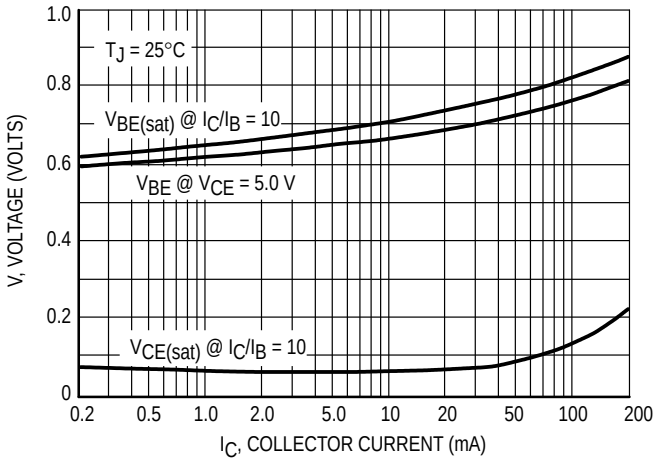


Figure 11. “On” Voltages

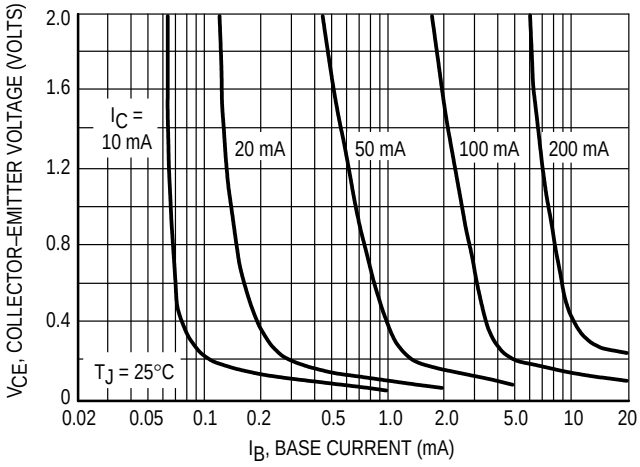


Figure 12. Collector Saturation Region

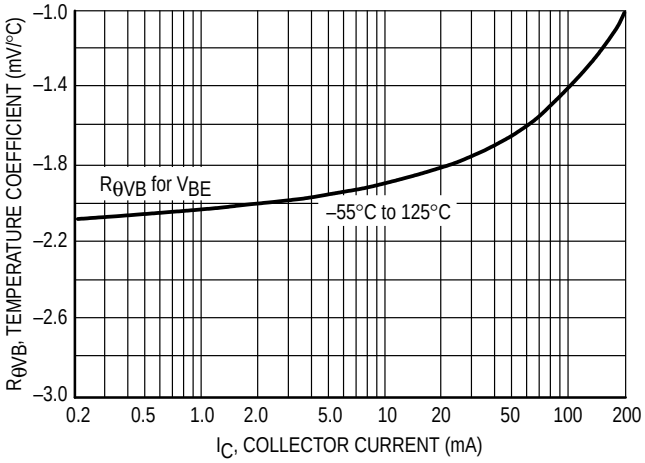
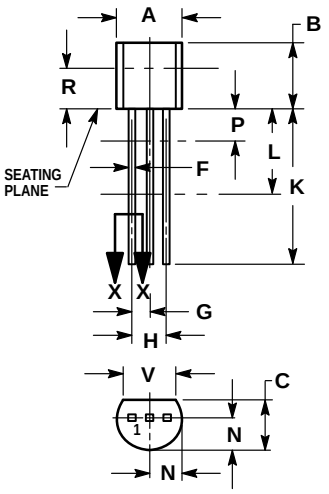
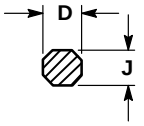


Figure 13. Base–Emitter Temperature Coefficient

PACKAGE DIMENSIONS





SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

CASE 029–04
(TO–226AA)
ISSUE AD

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

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